Shiro Hara, Ph.D
Representative of
Fab System Research Consortium, AIST, Japan.
Moore’s law

Semiconductor Shipment [million $/month]:
- 6.5X / Decade
- CAGR 20.5% / Year
- 1.7X / Decade
- CAGR 5.25% / Year

Compound Average Growth Rate (CAGR) [%]

World
- USA
- EU
- Japan
- Other

Moderate growth

Raw data was quoted from SIA Global Billing Report (1976-2010Apr).
Logistic Function

\[ N(t) = \frac{K}{1 + \left( \frac{K}{N(0)} - 1 \right) e^{-rt}} \]

for \( K = 1, \ r = 1, \ N(0) = 0.5 \)

Sigmoid Function

\[ N(t) = \frac{1}{1 + e^{-t}} \]
Simulation of Semiconductor Device market

- World-wide Device shipment [10 billion$/month]
- Year

Mature
- 100%
- 2nd Reform 80%

Mega Competition
- Linear Growth
- Exponential Growth
- Exponential Saturation
- 50% = maximum Growth rate

Free Growth
- 1st Reform 20%

1999.13

- Blue line is the curve fitting by logistic function.

- We’re here.

Approximately $290 billion/year (Saturation Value)

Revenue Growth
- Residual Growth: $38 billion (13%)

Exponential Growth
- Linear Growth

Exponential Saturation
Mass Production Users do not hope

Present Fab (Type1)

Users hope not only a low cost, but also a function that fits each user.

An Actual chip cost for a car is very high because of huge factory investment and low production volumes for cars.

It produces 500 million chips/year.

Suppliers can not deliver optimized functions and costs that users hope.

<table>
<thead>
<tr>
<th>Type</th>
<th>Quantity/year</th>
<th>Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Luxury cars</td>
<td>30,000</td>
<td>Poor Functions</td>
</tr>
<tr>
<td>Hybrid cars</td>
<td>500,000</td>
<td>Insufficient Inspection</td>
</tr>
<tr>
<td>Economy cars</td>
<td>120,000</td>
<td>Restricted Functions</td>
</tr>
</tbody>
</table>
Ideal Production for real user-needs

Minimal Fab (Type 2)

- Minimal waste
- Sufficient functions
- Low cost

Sufficient Functions with a low cost
Sufficient Inspection and Complete Functions for hybrids with a low cost
Sufficient Functions with low costs
7 Scaling down of fabrication factory

Traditional MAGA FAB

- Fab investment: 5B$
- 200m
- 2m

Room-sized Minimal FAB

- Fab investment: 0.5M$
- 10m
- 2m
- 0.3m

Minimal Manufacturing Technologies

- Saving energy & resources, cost, but high performance

No clean room

wafer size: 0.5”
Trend to enlarge silicon wafer

- 4” (1975~) 80 chips
- 6” (1980~) 180 chips
- 8” (1991~) 300 chips
- 12” (2001~) 1600 chips
- 18” (2020?)

Estimated by a chip size of 1cm²
1 product/min is our principle

TYPE 1

1 wafer/min

300mm wafer

1,000 chips/min

JISSO Processes

1,000 products/min

5:1&

1 body/min

1~10 parts/min

1 car/min

TYPE 2

1 wafer/min

half-inch wafer

1 chip/min

Transistor Processes

1 chip/min

JISSO Processes

Assembly

Fab System Research Consortium, AIST
Production types and product flows

Type 1  **Original Conveyor**
(Ford Production System)
- 1 product

Type 1’ **Present Conveyor**
- mixed flow
  for large production capacity

Type 2  **Minimal Manufacturing**
- minimal units
- Parallel lines
- Mono functional processes
- Cell production

※Note that this type 2 is totally different from Multi-functional Flexible Manufacturing System (FMS) that was remarkable before.

Production Speed:  Type 1 = Type 2 >> Type 1’
Assembly

Machining is high cost.

Machining is better.

(Dicing, Molding, Packaging, ...)

(Machining) (+MEMS)

Machining is must.

Wafer process

(Atom and Molecules)

Nanotechnology

Note that "Machining" here is Chambers for chemical processes, not mechanical machines.

Cell production system

World challenge:
Next production innovation for high-mix low volume but high-efficiency

Fabrication System Research Consortium, AIST
Reasonability of minimal type2

Basic Condition 1 process = 1min.

Production volume per month

= 1min x 60min x 24hours x 30days
= 43,200 products

• ~40,000 products/month
• ~500,000 products/year
Layouts of Minimal Systems

Test Fab

Mass production Fab

(For simple LSI process)
Business target

Production volume for a LSI [Log scale]

- Type 1
  - Suitable for Mega Production
  - Long Tail Business
  - Type 1'
- Mega Production
- Half-inch Business
  - Type 2
  - SoC / System LSI / Sensors / Controllers / etc.
- Potential Markets
- Test Samples

Variety of kinds

100B$ /year

Fab System Research Consortium, AIST
# Sizing effects of IC FAB

<table>
<thead>
<tr>
<th>Assumption</th>
<th>Present Mega FAB</th>
<th>Mini-fab (HALCA) project</th>
<th>Room-sized FAB</th>
<th>Desk-top FAB</th>
</tr>
</thead>
<tbody>
<tr>
<td>• cycle time=1min/wafer</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>• processes=500(metal 8 layers)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>• design rule=90nm</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Type of manufacturing processes</td>
<td>Present</td>
<td>Improved</td>
<td>Present</td>
<td>nanotech</td>
</tr>
<tr>
<td>Fab area</td>
<td>150m</td>
<td>30m</td>
<td>10m</td>
<td>1m</td>
</tr>
<tr>
<td>Wafer diameter</td>
<td>12&quot;</td>
<td>8&quot;</td>
<td>0.5&quot;</td>
<td>0.5&quot;</td>
</tr>
<tr>
<td>Chips/wafer (1chip=1cm²)</td>
<td>600</td>
<td>300</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Width of an equipment</td>
<td>3m</td>
<td>1m</td>
<td>30cm</td>
<td>-</td>
</tr>
<tr>
<td>number of Masks</td>
<td>34</td>
<td>34</td>
<td>Mask-less</td>
<td>Litho-less</td>
</tr>
<tr>
<td>number of Processes</td>
<td>600</td>
<td>500</td>
<td>350</td>
<td>32</td>
</tr>
<tr>
<td>Wafers of work in progress (wafers)</td>
<td>17,000</td>
<td>7,500</td>
<td>350</td>
<td>32</td>
</tr>
<tr>
<td>Number of equipment</td>
<td>300</td>
<td>100</td>
<td>350</td>
<td>32</td>
</tr>
<tr>
<td>Factory investment</td>
<td>5B$</td>
<td>0.1B$</td>
<td>0.5M$</td>
<td>450,000$</td>
</tr>
<tr>
<td>Equipment layout</td>
<td>Job</td>
<td>Job</td>
<td>Flow</td>
<td>Flow</td>
</tr>
<tr>
<td>Wafer operation rate (process time/total time)</td>
<td>~1%</td>
<td>~1%</td>
<td>40%</td>
<td>50%</td>
</tr>
<tr>
<td>Days for production</td>
<td>30 days</td>
<td>10 days</td>
<td>17 hours</td>
<td>32 hours</td>
</tr>
<tr>
<td>production capacity (300mm)</td>
<td>17,000</td>
<td>1,000</td>
<td>24</td>
<td>1</td>
</tr>
<tr>
<td>Year capacity (1cm² chip)</td>
<td>140million</td>
<td>7million</td>
<td>0.5million</td>
<td>8,400</td>
</tr>
<tr>
<td>Capacity for PC Mass product</td>
<td>70%</td>
<td>3.5%</td>
<td>0.1%</td>
<td>4x10⁻⁵</td>
</tr>
<tr>
<td>Sales</td>
<td>10B$</td>
<td>0.2B$</td>
<td>0.5M$</td>
<td>300,000$</td>
</tr>
<tr>
<td>Chip price (Sales / produced chip no.)</td>
<td>12$</td>
<td>29$</td>
<td>1.7$</td>
<td>36$</td>
</tr>
<tr>
<td>Efficiency of resources</td>
<td>0.1%</td>
<td>0.2%</td>
<td>0.2%</td>
<td>100%</td>
</tr>
</tbody>
</table>
Fab System Research Consortium

to create ideal fab-system in the 21st century

AIST Consortium

Fabrication System Research Consortium

Device makers/Minimal Fab Users
- Hitachi
- NEC
- Toshiba
- Sanyo Semiconductor manufacturing
- Omron
- Olympus
- Murata Manufacturing

Clean-room construction
- Taisei
- Asahikogyo sha

Back-end foundry
- Takashima

Equipment, Parts, materials
- Pre-tech
- Litho Tech Japan
- PMT
- Shin-Etsu Polymer
- Dainichi Sho ji
- JEM
- FUJI IMVAC

Fab-less
- Sanmei
- Okamoto Glass
- CKD
- Fujikin
- SHOEI Engineering
- Fujikoshi machinery
- Komatsu seiki Kosakusho

Logic Research

Solution
- JEDAT TOOL
- Uni3 system
- Asbil

University Public Sector
- Ochanimizu IPB
- TAKEWA PO
- KATO EML

AIST

Concept Technology

AIST

Minimal Manufacturing

Design
- Nanotech
- Design Network
- KOYU
- Unimac

Takashima Hitachi Toshiba Olympus Murata Manufacturing to create ideal fab-system in the 21st century